IN THE ABSTRACT:

Please amend the Abstract as follows:

~~According to the present invention, a memory circuit requiring refresh operations a first circuit which receives a command in synchronization with a clock signal, and which generates a first internal command internally and a second circuit which generates a second internal command, i.g. a refresh command, internally in a prescribed refresh cycle. And an internal circuit, according to said first internal command, executes corresponding control through clock-synchronous operations, and when said refresh command is issued, sequentially executes control corresponding to the refresh command and control corresponding to said first internal command through clock-asynchronous operations. According to the present invention, when a refresh timing signal is generated, the refresh operation can be intrupted among the external command operations~~ A memory circuit requiring refresh operations, the memory circuit includes a memory core having memory cells, and a memory control circuit which, for M external operation cycles, where M is greater than or equal to 2, has N internal operation cycles, where N is greater than M and less than 2M. The memory circuit also includes a refresh command generation circuit which generates refresh commands, and wherein the N internal operation cycles includes first internal operation cycles which execute external commands corresponding to the external operation cycles, and second internal operation cycles which execute the refresh commands, and the refresh command generation circuit generates the refresh commands according to a reception of the external command.